

Amendments to the Claims

1.-2. (Cancelled)

3. (Currently Amended) A semiconductor integrated circuit comprising:
~~pads;~~

~~a first power supply I/O cell which is connected to a first pad of said pads, said first pad being provided corresponding to said first power supply I/O cell;~~

~~a wire line that which is connected to said first power supply I/O cell;~~

~~a second power supply I/O cell which is connected to a second pad of said pads and is connected to said wire line to receive power supply from said first power supply I/O cell, said second pad being provided corresponding to said second power supply I/O cell and being, different from said first pad;~~

~~an internal cell; and~~

~~a power supply line which provides power supply to said internal cell, wherein said first power supply I/O cell and said second power supply I/O cell are being each connected to said power supply line[[,]];~~

~~wherein said first pad is connected to at least one external pin and wherein said second pad is not connected to any of the at least one external pin, and~~

~~wherein said second power supply I/O cell is not connected to the corresponding one of pads that corresponds to said second power supply I/O cell~~

pads which include a first pad and a second pad;

wherein said first pad is provided corresponding to said first power supply I/O cell,

wherein said second pad is provided corresponding to said second power supply I/O cell and is different from said first pad,

wherein said first pad is connected to said first power supply I/O and is connected to at least one external pin, and

wherein said second pad is not connected to said second power supply I/O and is not connected to any of the at least one external pin.

4. (Withdrawn) A method of designing a power supply layout of a semiconductor integrated circuit, comprising the steps of:

- identifying an unused I/O cell having no external connection; and
- assigning the I/O cell to be a power supply I/O cell having no direct external connection.

5. (Withdrawn) The method as claimed in claim 4, further comprising a step of connecting the power supply I/O cell to a power supply line for providing power supply to an internal cell and connecting the power supply I/O cell to a power supply I/O cell having direct external connection through a pad.

6. (Withdrawn) The method as claimed in claim 4, further comprising a step of identifying a portion that is lacking in a power supply current inside a chip, wherein

said step of assigning the I/O cell assigns the power supply I/O cell with respect to said portion.

7. (Withdrawn) The method as claimed in claim 6, wherein said step of identifying a portion that is lacking in a power supply current includes the steps of:

- obtaining first information about assignment of pins to I/O cells;
- obtaining second information about an amount of a necessary power supply current needed at each position inside the chip;
- calculating an amount of a provided power supply current in an initial state based on the first information; and
- comparing the calculated amount of a provided power supply current with the amount of a necessary power supply current indicated by the second information.

8. (Withdrawn) The method as claimed in claim 4, wherein said step of assigning the I/O cell includes a step of identifying the I/O cell to be assigned by use of a pointing device on a screen display that presents an illustration of a chip.

9. (Withdrawn) The method as claimed in claim 4, wherein said step of assigning the I/O cell includes a step of identifying the I/O cell to be assigned by specifying a number that has been allocated on the chip.

10-11. (Canceled)